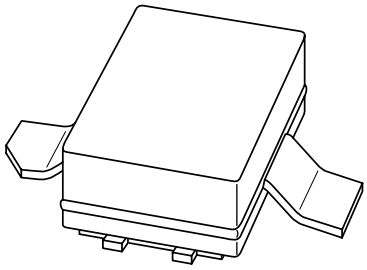
DATA SHEET



BLA1011-2
Avionics LDMOS transistor

Product specification
Supersedes data of 2002 Jun 17

2002 Oct 02

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Avionics LDMOS transistor BLA1011-2

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

APPLICATIONS

- Avionics applications in the 1030 to 1090 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to mounting base

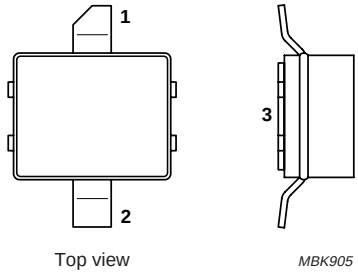


Fig.1 Simplified outline (SOT538A).

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)
Pulsed class-AB; t_p = 50 μs; δ = 2%	1030 to 1090	36	2	>16

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	2.2	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C	–	10	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}mb}$	thermal impedance from junction to mounting base	note 1	1	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	note 2	6.5	K/W

Notes

1. Thermal impedance is determined under RF operating conditions with pulsed bias and T_h = 25 °C.
2. Typical value for mounting on PCB with 32 0.4 mm thermal vias with 20 μm tin plating and thermal compound between PCB and heatsink.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.2 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 20 mA	2	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	0.1	mA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	2.8	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	40	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.75 A	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.75 A	–	1.2	–	Ω
C_{is}	input capacitance	V_{GS} = 0 V; V_{DS} = 26 V; f = 1 MHz	–	11	–	pF
C_{os}	output capacitance	V_{GS} = 0 V; V_{DS} = 26 V; f = 1 MHz	–	9	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 26 V; f = 1 MHz	–	0.5	–	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 6.5 K/W unless otherwise specified.

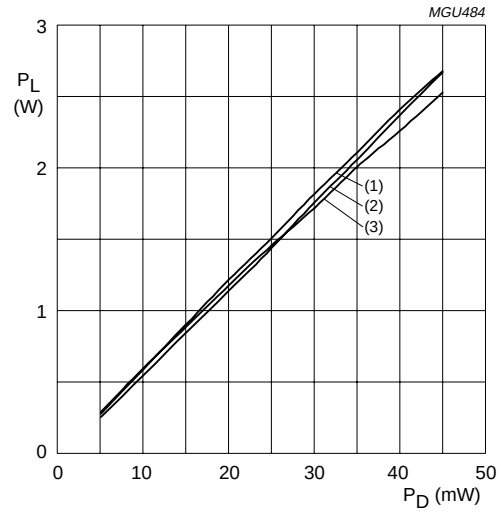
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	t_r (ns)	t_f (ns)	PULSE DROOP (dB)
Pulsed class-AB; t_p = 50 μs; δ = 2%	1030 to 1090	36	50	2	>16	<15	<15	<0.5

Ruggedness in class-AB operation

The BLA1011-2 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the operating conditions.

Typical impedance values

FREQUENCY (MHz)	Z_S (Ω)	Z_L (Ω)
1030	1.51 + j 11.76	6.9 + j 5
1060	1.51 + j 11.26	6.7 + j 5.9
1090	1.52 + j 10.77	5.1 + j 6.6



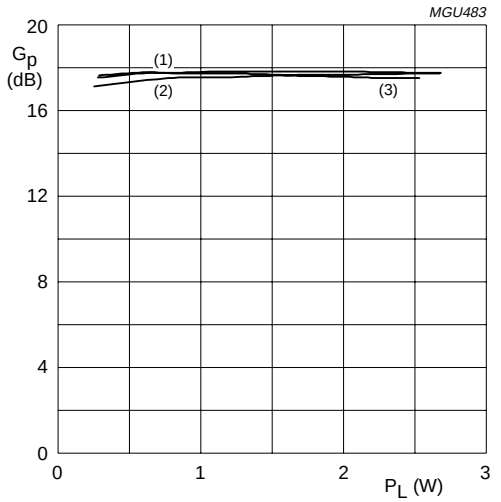
T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB;
t_p = 50 µs; δ = 2%.

(1) f = 1060 MHz.

(2) f = 1030 MHz.

(3) f = 1090 MHz.

Fig.2 Load power as a function of drive power; typical values.



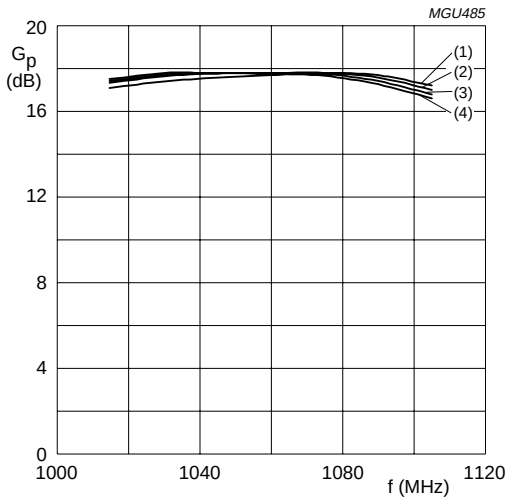
T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB;
t_p = 50 µs; δ = 2%.

(1) f = 1060 MHz.

(2) f = 1030 MHz.

(3) f = 1090 MHz.

Fig.3 Power gain as a function of load power; typical values.



T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB;
t_p = 50 µs; δ = 2%.

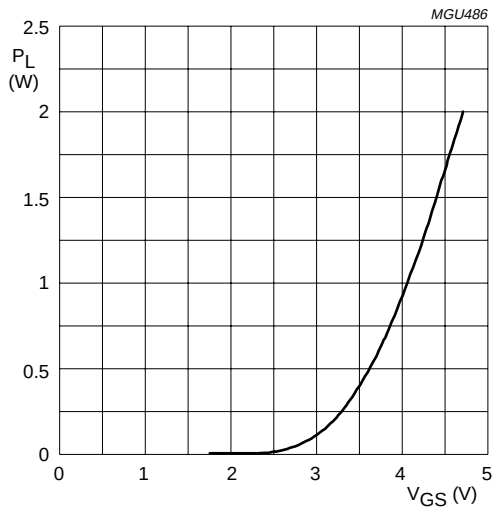
(1) P_L = 1 W.

(2) P_L = 2 W.

(3) P_L = 3 W.

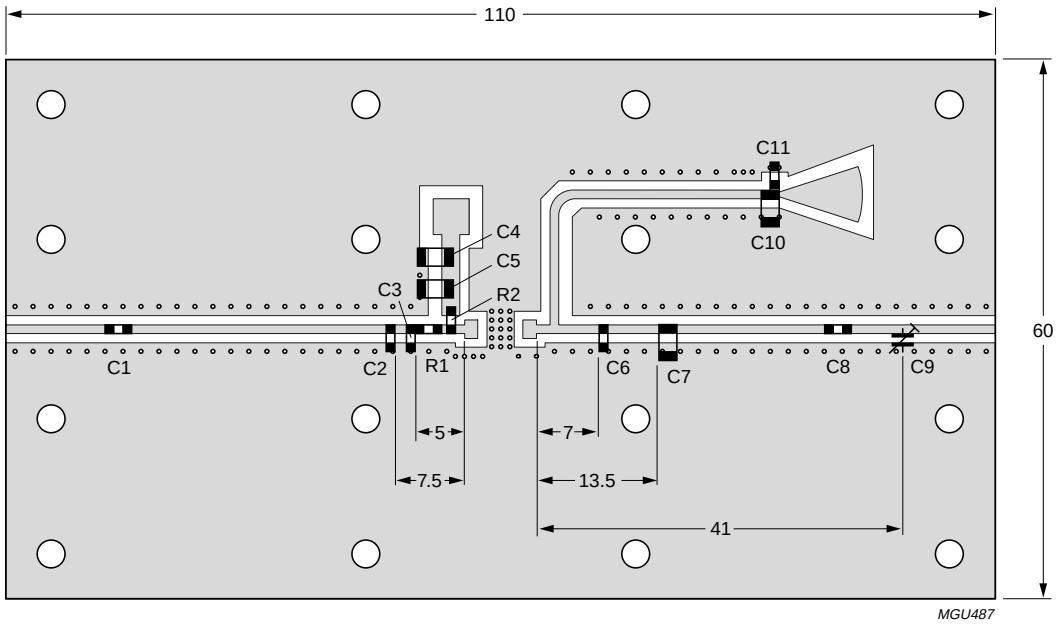
(4) P_L = 4 W.

Fig.4 Power gain as a function of frequency; typical values.



T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB;
f = 1090 MHz; t_p = 50 µs; δ = 2%.

Fig.5 Load power as a function of gate-source voltage; typical values.



Dimensions in mm.

The components are situated on one side of the Rogers 6010 printed-circuit board (thickness = 0.64 mm; ε_r = 6.2), the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through-metallization.

Fig.6 Printed-circuit board for class-AB test circuit.

List of components for class-AB test circuit (see Fig.6)

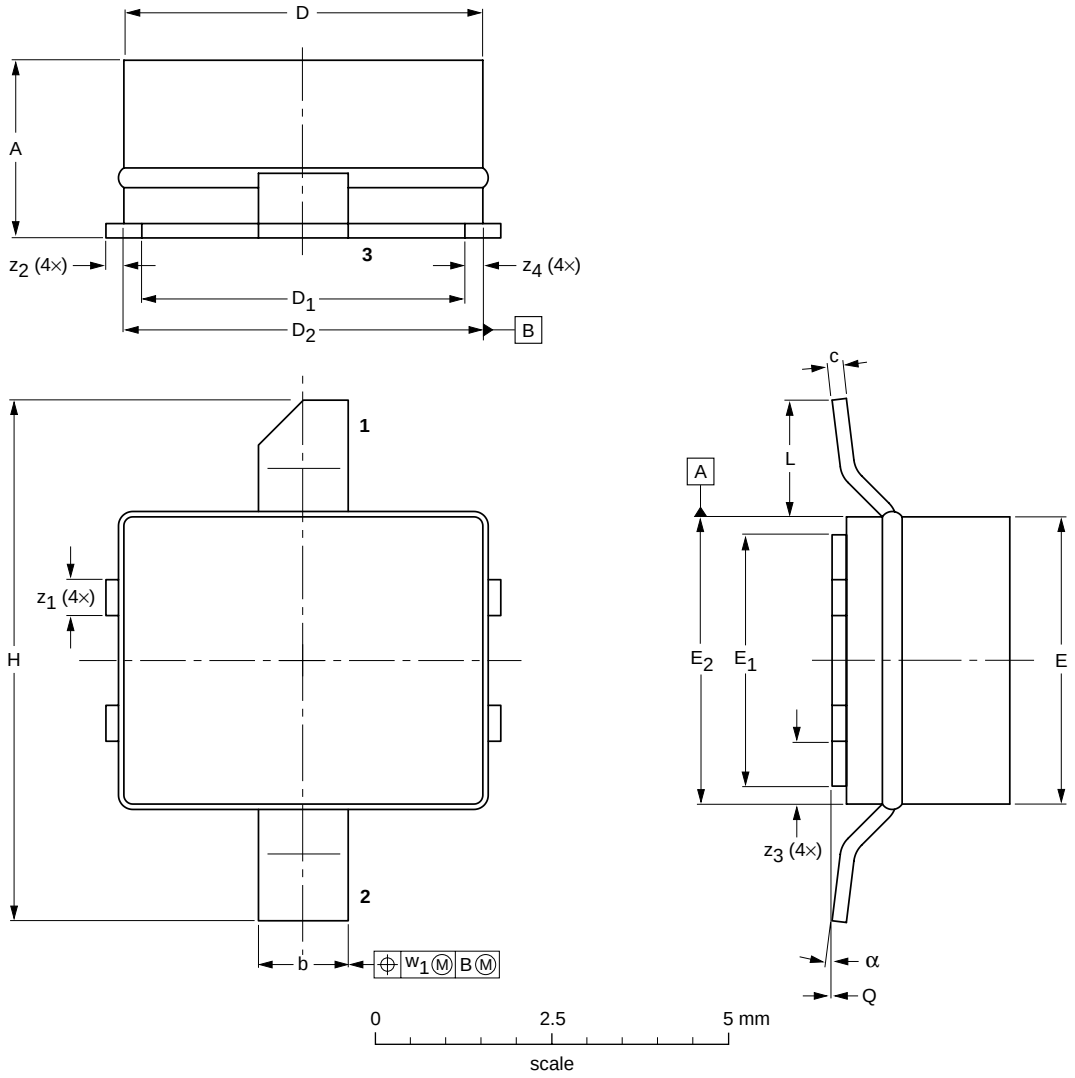
COMPONENT	DESCRIPTION	VALUE
C1, C8	multilayer ceramic chip capacitor; note 1	56 pF
C2	multilayer ceramic chip capacitor; note 1	7.5 pF
C3	multilayer ceramic chip capacitor; note 1	1.8 pF
C4, C10	multilayer ceramic chip capacitor; note 2	20 nF
C5	multilayer ceramic chip capacitor; note 3	33 pF
C6	multilayer ceramic chip capacitor; note 1	5.6 pF
C7	multilayer ceramic chip capacitor; note 3	6.2 pF
C9	tekelec trimmer; type 37283	0.4 to 2.5 pF
C11	multilayer ceramic chip capacitor; note 1	33 pF
R1	SMD resistor	2.2 Ω (2 in parallel)
R2	SMD resistor	22 Ω

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 200B or capacitor of same quality.
3. American Technical Ceramics type 100B or capacitor of same quality.

PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads **SOT538A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	Q	w_1	z_1	z_2	z_3	z_4	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.16 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	0.58 0.43	0.25 0.18	0.97 0.81	0.51 0.00	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.203 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	0.023 0.017	0.010 0.007	0.038 0.032	0.020 0.000	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT538A						~~00-03-03~~ 02-08-20

DATA SHEET STATUS

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